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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,865	12/12/2003	Soon-Yong Kweon	51876P424	1525
8791	7590	06/23/2004	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025			CHEN, JACK S J	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/734,865

Applicant(s)

KWEON, SOON-YONG

Examiner

Jack Chen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/12/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

In response to the communication filed on December 12, 2003, claims 1-7 are active in this application.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement filed on December 12, 2003 has been considered.

Oath/Declaration

Oath/Declaration filed on December 12, 2003 has been considered.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Melnick et al., U.S./5,998,258.

Melnick et al. discloses a method fabricating a ferroelectric memory device, which comprises forming a first insulation layer 220 on a substrate 210 (fig. 2); forming storage node contact 216 contacting partial portion of the substrate by passing through first insulation layer (fig. 2); forming stack pattern of a lower electrode 610/612 contacting storage node contact and a hard mask 614 on the first insulation layer (fig. 6); forming a second insulation layer 420 on an entire surface of the resulting structure including the stack pattern (fig. 4); planarizing the second insulation layer until surface the hard mask is exposed (fig. 6); removing selectively exposed hard mask make surface level of the lower electrode lower than that the second insulation layer (fig. 7); and forming sequentially a ferroelectric layer 810 and an upper electrode 812 (fig. 8) on second insulation layer and the lower electrode, see figs. 1-10; cols. 1-8 for more details.

Re claim 2, wherein the hard mask is made of TiN, TaN (fig. 6; col. 4, lines 1-6).

Re claim 3, inherently shows the step of making the surface level of the lower electrode lower than that of the second insulation layer proceeds by performing a wet etching process or a dry etching process to the hard mask (fig. 7; col. 4, lines 1-32).

Re claim 6, wherein the step of planarizing the second insulation until the surface of the hard mask is exposed includes the steps of planarizing a partial portion of the second insulation layer by performing a chemical mechanical polishing (CMP) process; and performing an etch-back process to the second insulation layer to make the hard mask exposed (col. 4, lines 20-42).

Re claim 7, wherein the step of planarizing the second insulation layer until the surface of the hard mask is exposed proceeds by applying a CMP process or an etch-back process at once to the second insulation layer (col. 4, lines 20-45).

4. Claims 1, 3 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Graettinger et al., U.S./5,843,830.

Graettinger et al. discloses a method fabricating a ferroelectric memory device, which comprises forming a first insulation layer 36 on a substrate 30 (fig. 2); forming storage node contact 38 (fig. 2) contacting partial portion of the substrate by passing through first insulation layer; forming stack pattern of a lower electrode 50/60 contacting storage node contact and a hard mask 70 (fig. 5) on the first insulation layer; forming a second insulation layer 80 (fig. 6) on an entire surface of the resulting structure including the stack pattern (fig. 6); planarizing the second insulation layer until surface the hard mask is exposed (fig. 7); removing selectively exposed hard mask make surface level of the lower electrode lower than that the second insulation layer (fig. 8); and forming sequentially a ferroelectric layer 90 and an upper electrode 100 (fig. 10) on second insulation layer and the lower electrode, see figs. 1-10; cols. 1-8 for more details.

Re claim 3, wherein the step of making the surface level of the lower electrode lower than that of the second insulation layer proceeds by performing a wet etching process or a dry etching process to the hard mask (fig. 8; col. 5, lines 1-15).

Re claim 7, wherein the step of planarizing the second insulation layer until the surface of the hard mask is exposed proceeds by applying a CMP process or an etch-back process at once to the second insulation layer (fig. 7, col. 4, line 66 to col. 5, line 15).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Melnick et al., U.S./5,998,258 in view of Wang et al., U.S. Pub. No. 2002/0045344 A1 or Gupta et al., U.S./6,225,202 B1.

Melnick et al. Disclosed above ; however, Melnick et al. is silent to using sulfuric acid and hydrogen peroxide in a ratio of about 4 to about 1 or SC-1 to remove the hard mask (i.e., TiN).

Wang et al. Teaches a method for forming a semiconductor device, which includes using sulfuric acid and hydrogen peroxide in a ratio of about 4 to about 1 to remove TiN (see paragraph 0056).

Gupta et al. Also teaches a method for forming a semiconductor device, which includes using SC-1 to remove TiN (col. 2, line 59 to col. 3, line 15 and col. 1, lines 10-27). Further in this regard, with respect to claim 4, claimed ranges of etchant ratio, absent evidence of disclosure of criticality for the range giving unexpected results are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller 105 USPQ233, 255 (CCPA 1955)*, the selection of reaction parameters such as temperature, ratio and concentration would have been obvious. *See also In re Waite 77 USPQ*

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586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmischer 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use sulfuric acid and hydrogen peroxide in a ratio of about 4 to about 1 to remove TiN as taught by Wang et al. or SC-1 to remove TiN as taught by Gupta et al. in the method of Melnick et al. in order to selectively remove the hardmask.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Melnick et al., U.S./5,998,258 in view of Kobayashi, U.S./6,610,597 B2 or Gupta et al., U.S./6,225,202 B1.

Melnick et al. Disclosed above ; however, Melnick et al. is silent to using argon and chlorine to remove the hard mask (i.e., TiN).

KobayashiTeaches a method for forming a semiconductor device, which includes using argon and chlorine to remove TiN (col. 4, lines 30-50).

Gupta et al. Also teaches a method for forming a semiconductor device, which includes argon and chlorine to remove TiN (col. 2, line 59 to col. 3, line 15).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use argon and chlorine to remove TiN as taught by Kobayashi or Gupta et al. in the method of Melnick et al. in order to selectively remove the hardmask.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graettinger et al., U.S./5,843,830 in view of Kang, U.S./5,786,259.

Graettinger et al. Disclosed above ; however, Graettinger et al. is silent to using TiN as the hard mask.

Kang teaches a method for forming a semiconductor device, which includes using TiN or silicon nitride as the hard mask 217 (fig. 13) for the lower electrode 213/215 (figs. 14-15) in order to eliminate the damage to and/or consumption of the lower electrode during the step of etching the insulating layer, see figs. 1-18; cols. 1-10 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use either TiN or silicon nitride for the hardmask as taught by Kang in the method of Graettinger et al. in order to eliminate the damage to and/or consumption of the lower electrode during the step of etching the insulating layer.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graettinger et al., U.S./5,843,830 in view of Wang et al., U.S. Pub. No. 2002/0045344 A1 or Gupta et al., U.S./6,225,202 B1.

Graettinger et al. Disclosed above ; however, Graettinger et al. is silent to using sulfuric acid and hydrogen peroxide in a ratio of about 4 to about 1 or SC-1 to remove the hard mask (i.e., TiN).

Wang et al. Teaches a method for forming a semiconductor device, which includes using sulfuric acid and hydrogen peroxide in a ratio of about 4 to about 1 to remove TiN (see paragraph 0056).

Gupta et al. Also teaches a method for forming a semiconductor device, which includes using SC-1 to remove TiN (col. 2, line 59 to col. 3, line 15 and col. 1, lines 10-27). Further in

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this regard, with respect to claim 4, claimed ranges of etchant ratio, absent evidence of disclosure of criticality for the range giving unexpected results are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller* 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature, ratio and concentration would have been obvious. See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use sulfuric acid and hydrogen peroxide in a ratio of about 4 to about 1 to remove TiN as taught by Wang et al. or SC-1 to remove TiN as taught by Gupta et al. in the method of Graettinger et al. in order to selectively remove the hardmask.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graettinger et al., U.S./5,843,830 in view of Kobayashi, U.S./6,610,597 B2 or Gupta et al., U.S./6,225,202 B1.

Graettinger et al. Disclosed above ; however, Graettinger et al. is silent to using argon and chlorine to remove the hard mask (i.e., TiN).

KobayashiTeaches a method for forming a semiconductor device, which includes using argon and chlorine to remove TiN (col. 4, lines 30-50).

Gupta et al. Also teaches a method for forming a semiconductor device, which includes argon and chlorine to remove TiN (col. 2, line 59 to col. 3, line 15).

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use argon and chlorine to remove TiN as taught by Kobayashi or Gupta et al. in the method of Graettinger et al. in order to selectively remove the hardmask.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graettinger et al., U.S./5,843,830 in view of Mikawa et al., U.S. Pub. No. 2004/0053466 A1.

Graettinger et al. Disclosed above ; however, Graettinger et al. is silent to using CMP in combination with etch-back process for planarizing the second insulation layer.

Mikawa et al. teaches a method for forming a semiconductor device, which includes using CMP in combination with etch-back process for planarizing the insulation layer (figs. 1F-1G; paragraph 56) in order to eliminate the micro-scratches due to the CMP process.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use CMP in combination with etch-back process for planarizing the insulation layer as taught by Mikawa et al. in the method of Graettinger et al. in order to eliminate the micro-scratches due to the CMP process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jack Chen
Primary Examiner
Art Unit 2813